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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,413	03/10/2004	Xiangfeng Duan	2132.0180000	9041

33140 7590 11/02/2006

NANOSYS INC.
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EXAMINER	
REAMES, MATTHEW L	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,413	DUAN ET AL.	
	Examiner	Art Unit	
	Matthew L. Reames	2891	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-24,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/5/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Bawendi (US 20050072989).

a. As to claim 1, Bawendia teaches a MOSFET structure (see fig. 2 with a nanoelement film covered with a functional group (see floating gate and paragraph 43). Wherein the functional group increase the solubility of the the nanoelements (see paragraph 43).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2,6-24,26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flagan in view of Hutchinson.

a. As to claims 1,2,26,27 Flagan teaches a memory device, comprising: a substrate; a source region of said substrate; a drain region of said substrate; a channel region between said source and drain regions; a thin film of nanoelements on said channel region; and a gate contact formed on said thin film of nanoelements (see fig. 11, and abstract). 9

Hutchison teaches using a spacer group on nanostructures for nanostructure-nanostructure spacing (paragraph 20).

It would have been obvious to one of ordinary skill in the art to use a siloxane chemistry to form a spacer group on the silicon nanoparticles to orient the nanoparticles. Further this would inherently increase the soluble.

One would have been so motivated in order precise spacing of the nanoparticles as taught by Hutchinson (see paragraph 20).

b. As to claim 6, Flagan teaches a device further comprising: a dielectric layer between said substrate and said thin film of nanoelements (fig. 11 item 124).

c. As to claim 7, Flagan teaches a device further comprising: a dielectric layer between said thin film of nanoelements and said gate contact (see fig. 11 item 128).

d. As to claim 8, Flagan further teaches, each nanocrystal has a core, and a shell that surrounds said core (see fig. 6).

e. As to claim 9, Flagan teaches a shell made from oxide (see fig. 6 item 106).

f. As to claim 10, Flagan teaches herein said thin film of nanoelements includes nanoelements having a plurality of charge injection threshold voltages, wherein said memory device is a multistate memory device (see fig. 14, and paragraph 63), the threshold voltage varies with time therefore the nanoelements voltages vary with time.

g. As to claim 11, Flagan teaches each nanocrystal has a core, and a shell that surrounds said core (see fig. 6).

h. As to claim 12, Flagan teaches a shell made from oxide (see fig. 6 item 106).

i. As to claim 13, Flagan teaches , wherein a first plurality of nanoelements of said thin film of nanoelements have shells formed to have a first thickness to cause said first plurality of nanoelements to have a first charge injection threshold voltage; and a second plurality of nanoelements of said thin film of nanoelements have shells formed to have a second thickness to cause said second plurality of nanoelements to have a second charge injection tllreshold voltage (see paragraph 56). Wherein the first shell is equal to the second shell thickness, but the size varies at a log-normal which would inherently change the injection voltage.

j. As to claim 14, Flagan does not explicitly state a plurality shell thicknesses. However, do to the method of manufacture the shell will inherently have different thicknesses. The shell thicknesses will inherently be described by a normal distribution, with a mean and some standard deviation. Moreover with a

plurality of the shell thicknesses, there will be a plurality injection of injection voltages since the injection voltage depend on the shell thickness.

k. As to claims 15,16,42,43,46, Flagan teaches a memory device wherein said nanoelements have a plurality of sizes to cause said nanoelements to have said plurality of charge injection threshold voltages (paragraph 56, log-normal), where since the size change the injection voltage inherently changes. Flagan further teaches wherein said plurality of sizes corresponds to a plurality of capacitance values for said nanoelements, (paragraph 56) where the size changes inherently changes the capacitance.

l. As to claim 17-19,44, Flagan teaches wherein he memory device of claim 10, wherein discrete numbers of electrons are injected into said nanoelements according to the Coulomb blockade effect to have said plurality of charge injection threshold voltages (see paragraph 5). Flagan teaches wherein said nanoelements are quantum dots (see paragraph 5 and 6) and inherently due to the size has quantum confinement with discrete states for each nanoparticle (paragraph 6).

m. As to claim 21, Flagan teaches an N-MOS (see paragraph 37).

n. As to claim 22,23,24,45 Flagan teaches a monolayer (paragraph 54) a sub-monolayer (paragraph 54), plurality of nanoelement layers

2. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Flagan/Hutchinson.

a. Flagan teaches a N-MOS floating gate structure. Further it is well known in the art that quantum effect i.e. confinement work equally well for electron and holes. Moreover P-MOS are well known in the art, used in conjunction with memory devices. Flagan does not explicitly teach a P-MOS structure.

However it would have been obvious to one of ordinary skill in the art at the time of the invention to have formed said device as a P-MOS structure.

One would have been so motivated in order to use this memory device with a P-MOS device in a memory array.

4. Claim 1,3,4,5,23 rejected under 35 U.S.C. 103(a) as being anticipated by Dai in view of Hutchinson.

a. As to claims 1,3,4, Dai teaches a memory device, comprising: a substrate; a source region of said substrate; a drain region of said substrate; a channel region between said source and drain regions; a thin film of nanoelements on said channel region; and a gate contact formed on said thin film of nanoelements (see fig. 1). Further Dai, teaches that these are carbon nanotubes/nanowire/nanorods (see abstract). According to applicant's Specification there is no difference between a nanowire and nanorod.

Hutchison teaches using a spacer group on nanostructure-nanostructure spacing (paragraph 20).

It would have been obvious to one of ordinary skill in the art to use a form a spacer group on the nanorods/wires of Dai to orient the nanorods/wires. Further this would inherently increase the soluble.

One would have been so motivated in order precise spacing of the nanorods/wires as taught by Hutchinson (see paragraph 20).

b. As to claim 23, Dai teach a plurality of layers (see fig. 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew L. Reames whose telephone number is (571)272-2408. The examiner can normally be reached on M-Th 6:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MLR

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER